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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,442	02/11/2002	Robert Allan Whitton	0808.65530	4484

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,442	WHITTON, ROBERT ALLAN	
	Examiner	Art Unit	
	Kenneth Tang	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/11//02.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/11/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 recites the limitation "the last thread" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9, 11, 13-14, 16-18, 20-23, and 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Zahir et al. (hereinafter Zahir) (US 6,065,114).

3. As to claim 1, Zahir teaches a processor switchable between a first execution mode and a second execution mode (context switching between nodes), the processor having a first processor context (first context) when in the first execution mode and a second processor context (second

context or target context), different from the first processor context (context A compared to context B), when in the second execution mode, wherein the processor is arranged to generate an exception (interrupt) when the processor attempts to change (switching) from one execution mode to the other *(col. 8, lines 59- col. 9, lines 1-19, col. 10, lines 13-31, col. 11, lines 7-37 and claim 1)*.

4. As to claim 2, Zahir teaches wherein the second processor context is larger than the first processor context and the exception is generated when the processor attempts to change from the first execution mode to the second execution mode (the context of BSPLOAD is smaller than PTR or the context of BSPLOAD is larger than PTR) *(col. 14, lines 35-65)*.

5. As to claim 3, Zahir teaches wherein the processor is arranged to preserve the second processor context (store a content of a second register), or that part of the second processor context which is different from the first processor context, when said exception has been generated (interrupt from interrupt handler) *(see Abstract, col. 1, lines 61-68 through col. 2, lines 1-10, col. 10, lines 13-31)*.

6. As to claim 4, Zahir teaches wherein the processor is arranged to execute a plurality of threads on a time share basis (parallel, etc.), and the processor is arranged such that when the processor is switched to a thread which is in the first execution mode, or when the processor is switched to a thread which was the last thread to be in the second execution mode (context switching), and it is inherent that only the first processor context is preserved. Silberschatz's

OPERATING SYSTEM CONCEPTS (4.2.3 Context Switch, page 97) shows that the standard definition of context switching requires saving the state of the old process and loading the saved state for the new process.

7. As to claim 5, Zahir teaches wherein the second processor context, or that part of the second processor context which is different from the first processor context (context A compared to context B), preserved when the processor next enters the second execution mode to execute a thread other than the last thread to be in the second execution mode (second portion/content/register is reserved/saved/stored) *(see Abstract and col. 1, lines 61-67 hrough col. 2, lines 1-8)*.

8. As to claim 6, Zahir teaches wherein the processor is arranged to execute a plurality of threads on a time share basis (concurrent execution, operating in parallel) *(col. 1, lines 44-57)*, and it is inherent that the number of threads that may be in the second execution mode at any one time is less than the total number of threads that may be active on the processor at any one time because it is not possible for the number of threads in any mode to exceed the total number of threads.

9. As to claim 7, Zahir teaches wherein the processor is arranged such that, when said exception has been generated, a check is carried out to determine whether the thread that caused the exception is allowed to enter the second execution mode (the interrupt handler provides the controls for the interrupts) *(col., 12, lines 22-36, etc.)*.

10. As to claim 8, Zahir teaches wherein the check comprises determining whether that thread is a thread which is barred (ignored or barred by the interrupt handler if the bit is not set) from the second execution mode *(col. 11, lines 51-65)*.

11. As to claim 9, Zahir teaches wherein the check (interrupt handler) comprises determining whether a predetermined number of other threads are already in the second execution mode (data table information) *(col. 11, lines 7-22)*.

12. As to claim 11, Zahir teaches wherein the processor is arranged to execute a first instruction set when in the first execution mode and a second instruction set when in the second execution mode *(see Abstract and col. 8, lines 4-32)*.

13. As to claim 13, Zahir teaches the processor comprising at least one execution unit and a plurality of storage locations (backing store in memory and registers), the first processor context comprising the contents of storage locations accessible in first execution mode and the second processor context comprising the contents of storage locations (first register and second register) accessible in the second execution mode *(see Abstract and col. 1, lines 61-67 through col. 2, lines 1-9)*.

14. As to claim 14, Zahir teaches the processor comprising a plurality of computational units for executing instructions in parallel, each computational unit having at least one execution unit

and at least one storage location to which the execution unit has access (backing store in memory and registers) *(col. 1, lines 44-58)*.

15. As to claim 16, it is rejected for the same reasons as stated in the rejection of claims 1 and 4.

16. As to claim 17, it is rejected for the same reasons as stated in the rejection of claim 5.

17. As to claim 18, it is rejected for the same reasons as stated in the rejection of claim 6.

18. As to claim 20, it is rejected for the same reasons as stated in the rejections of claims 1 and 6.

19. As to claim 21, it is rejected for the same reasons as stated in the rejections of claim 7.

As to claims 22-23, they are rejected for the same reasons as stated in the rejection of claims 8-9.

As to claims 25-27, they are rejected for the same reasons as stated in the rejection of claims 1, 16, and 20.

As to claims 28-30, they are rejected for the same reasons as stated in the rejection of claims 25-27.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Flynn et al. (hereinafter Flynn) (US 6,052,708).

21. As to claim 10, Zahir fails to explicitly teach wherein the processor is arranged such that, if a predetermined number of other threads are already in the second execution mode, execution of the thread that caused the exception is suspended until the number of other threads that are in the second execution mode is less than the predetermined number. However, Flynn teaches suspending the execution of the switch until a predetermined number of instructions have been executed in the active thread *(col. 6, lines 46-65)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of suspending the execution of the switch until a predetermined number of instructions have been executed in the active thread to the existing system of Zahir because one of ordinary skill in the art of context switching would know that it would provide a control for context switching.

22. As to claim 24, it is rejected for the same reasons as stated in the rejections of claim 10.

23. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Ackerman et al. (hereinafter Ackerman) (US 5,481,719).

As to claim 12, Zahir fails to explicitly teach teaches wherein the processor is switchable between a supervisor mode and a user mode, the user mode having restricted access to the processor's resources in comparison to the supervisor mode, and, when said exception is generated, the processor transfers from the user mode to the supervisor mode. However, Ackerman teaches switching based on exceptions/interrupts between a supervisor mode and a user mode, whereby the user mode not having as much privileges as the supervisor mode *(col. 20, lines 27-33, col. 13, lines 18-27)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of the user mode and supervisor mode because the various levels of privileges increase the security of the system *(col. 2, lines 23-25)*.

24. **Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Spiller (US 6,047,122).**

25. As to claim 15, Zahir fails to explicitly teach wherein the first execution mode is a scalar mode and the second execution mode is a parallel mode. However, Spiller teaches switching from a scalar mode to a parallel mode *(col. 4, lines 1-17 and see claim 1)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of switching from a scalar mode to a parallel mode because it would increase the speed of processing *(col. 2, lines 1-8)*.

26. As to claim 19, it is rejected for the same reasons as stated in the rejection of claim 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
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